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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,891	04/16/2004	Remi LeReverend	ZLINK.026A	1422

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,891	LEREVEREND, REMI	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-9 rejected under 35 U.S.C. 102(b) as being anticipated by Soumyanath et al. (U.S. Patent No. 6,218,892). With regard to Claim 1, Soumyanath discloses a circuit comprising at least one MOS transistor (M3) and external circuitry (differential amplifier 12 and body control circuitry 30) to forward bias a well of said MOS transistor (M1) (column 3, lines 59-60), a method of biasing said well comprising: determining a bias current to be drawn from said well (column 5, lines 36-52) from said well with said external circuitry (differential amplifier 12 and body control circuitry 30).

With regard to Claims 2 and 3, Soumyanath discloses external circuitry comprising a transistor and a differential amplifier (column 3, lines 12-16).

With regard to Claim 4, Soumyanath discloses on figures 1 and 5 a first MOS transistor (M1) formed in a well and comprising a gate terminal configured as a first input to a differential amplifier (12) and a source terminal; a second MOS transistor (M2) formed in a well and comprising a gate terminal configured as a second input to the differential amplifier (12), and a source terminal coupled to said source terminal of said first MOS transistor (M1), wherein said

well of said first MOS transistor (M1) is coupled to said well of said second MOS transistor (M2), a third MOS transistor (Load L1) comprising a source terminal coupled to a voltage source (Vcc) and a drain coupled to said source terminals of said first (M1) and second (M2) MOS transistors and a transistor current source (body control circuitry 30) coupled to at least said well of said first MOS transistor (M1) so as to draw current from said well.

With regard to Claim 5, Soumyanath discloses on figures 1 and 5 a transistor current source (body control circuitry 30) coupled to at least said well of said second MOS transistor (M2) so as to draw current from said well.

With regard to Claim 6, Soumyanath discloses on figures 1 and 5 discloses a circuit comprising two or more transistors (M1, M2, M3) formed in wells coupled to different biasing circuits, wherein a current drawn from the wells is substantially the same and wherein the well potentials are different.

With regard to Claim 7, Soumyanath discloses at least one of said biasing circuits (30) comprises a transistor coupled to at least one of the wells and configured to raw a current from the well.

With regard to Claim 8, Soumyanath discloses a method of reducing the operating voltage level of an integrated circuit comprising at least one group of two or more transistors (M1, M2, M3), wherein said transistors are formed in wells (figure 5), said method comprising forward biasing said transistor wells with a common current but not a common potential (Vcc, Vin+).

With regard to Claim 9, Soumyanath discloses a plurality of MOS transistors (M1, M2,M3) comprising wells (figure 5), wherein the wells are connected to current sources (figure 1) and the current sources are configured to forward bias said wells by drawing substantially the same current from said wells. It is noted that the limitations "fabricated' from a series of different wafers subject to process variations during wafer production" and 'irrespective of any resulting inter-wafer or intra-wafer differences in the source to well voltage produced by said current due to process variations affecting the physical structure of the MOS transistors within or between wafers", are process limitations that do not distinguish the claimed invention from that taught by Soumyanath.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U 2815
9/30/05

JEROME JACKSON
PRIMARY EXAMINER